

AMENDMENTS

Please amend the application as indicated hereafter.

In the Claims

Please cancel claim 3 ~~without~~ without prejudice, waiver or disclaimer.

Please substitute the following clean copy text for the pending claims, of the same number.

01 1. (Twice Amended) An integrated circuit comprising:
a first port for outputting a signal;
a second port for receiving said signal;
a common area comprising an alignment link for electrically connecting said first port with said second port;
said first port is directly and electrically connected to said alignment link from a first area without the use of a first linking area that includes bridging traces for linking mis-aligned ports with said first port and said common area;
said second port is directly and electrically connected to said alignment link from a second area without the use of a second linking area that includes bridging traces for linking mis-aligned ports with said second port and said common area; and
said alignment link comprises a signal buffer for buffering a signal traveling along said alignment link between said first port and said second port; said alignment link is arranged within said common area.

02 6. (Twice Amended) An integrated circuit comprising:
a first port located in a first area of integrated circuit real estate, for outputting a signal;
a second port located in a second area of integrated circuit real estate, for receiving said signal;
a common area comprising an alignment link for electrically connecting said first port with said second port;
said first port is directly and electrically connected to said alignment link from a first area without the use of a first linking area that includes bridging traces for linking mis-aligned ports with said first port and said common area;

D2
concl'd

said second port is directly and electrically connected to said alignment link from a second area without the use of a second linking area that includes bridging traces for linking mis-aligned ports with said second port and said common area;

said alignment link comprises a signal buffer for buffering a signal traveling along said alignment link between said first port and said second port; and

said integrated circuit real estate comprises multi-levels.

D3

17. (Twice Amended) An integrated circuit comprising:

a first port for outputting a signal;

a second port for receiving said signal;

a common area comprising an alignment means for electrically connecting said first port with said second port;

said first port is directly and electrically connected to said alignment means from a first area without the use of a first linking area that includes bridging traces for linking mis-aligned ports with said first port and said common area; and

said second port is directly and electrically connected to said alignment means from a second area without the use of a second linking area that includes bridging traces for linking mis-aligned ports with said second port and said common area.

D4

21. (Newly Added) A buffering circuitry with aligning ports that share a common area of integrated circuit real estate, said buffering circuitry comprising:

a first area arranged on a wiring level of said integrated circuit real estate, said first area includes a set of output ports;

a common area that is arranged in multilevel of said integrate circuit real estate, said common area includes signal buffering blocks provided on a semiconductor level, said common area also includes a first set and a second set of wiring traces provided in said wiring level said common area is arranged so as to allow for placement of said first and second sets of wiring traces to be within said common area, wherein said set of output ports is electrically connected to said first set of wiring traces of said signal buffering blocks without the use of a first linking area that includes bridge traces for linking mis-aligned ports with said first port and said common area; and

a second area arranged on said wiring level of said integrated circuit real estate, said second area includes a set of input ports that is electrically connected to said second set of

D4
conced

wiring traces of said signal buffering blocks without the use of a second linking area that includes bridge traces for linking mis-aligned ports with said second port and said common area.
